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List of published papers in national/ international conference proceedings during the year 2018

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A Novel Transformerless Asymmetrical Fifteen Level Inverter Topology for Renewable Energy Applications

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S. Chaitanya ; N. Rajanand Patnaik ; Ch. B. A. Raju All Authors

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In the field of medium and high power applications Multilevel Inverter (MLI) topology is an alternative concept. It has the capability to generate the high voltage staircase pseudo-sinusoidal waveform with less distortion and high quality. But it requires more number of Switching Components (SC) with complex PWM (Pulse Width Modulation) strategies hence the cost and size of inverter becomes high. So, in view of this authors investigated a novel asymmetrical transformerless MLI topology of fifteen level inverter is presented in this paper, with an attempt of reduction in overall device count (switches, diodes, capacitors, dc voltage sources, etc.,) compared to all existing multilevel inverters. The basic structure and operating modes of proposed MLI is explained clearly. It requires seven power switches (IGBT), three diodes and three DC-bus capacitors are required to generate fifteen level 1-Φ voltage. Furthermore, an efficient PWM technique is implemented with seven reference signals whose magnitude is equal to carrier signal. The performance of proposed MLI is accomplished in terms of Total Harmonic Distortion (THD) at modulation index M=0.9. The evaluation of MLI is carried out through MATLAB/SIMULINK environment.

Published in: 2018 Fourth International Conference on Advances in Electrical, Electronics, Information, Communication and Bio-Informatics (AEEICB)

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Capacitor Voltage Balancing for Five-Level Neutral-Point Clamped Inverter using Modified Carrier Waves for Carrier-Based PWM Technique

2019 IEEE 16th India Council International Conference (INDICON)

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IECON 2014 - 40th Annual Conference of the IEEE Industrial Electronics Society

Published: 2014

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INSPEC Accession Number: 18133590

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S. Chaitanya
Department of EEE, Govt Engg College, Bharatpur, India

N. Rajanand Patnaik
G. S. Electricals, Vijayawada, AP, India

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Department of EEE, AEC, Kakinada, Surampalem, India

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In microprocessors, digital signal processors, various kinds of arithmetic building blocks such as adder/substractor, multiplier/divider, shifter are required to compute binary data. The priority of datapath can be operation speed, low power consumption, area or design time. The most important design goals in many cases are high operation speed and low power consumption. The basic structure in any arithmetic block is an adder circuit. Hence, by optimising the adder circuit, high oparation speed and low power consumption can be achieved. Several kinds of adders have been proposed to reduce the worst-case propagation delay from Least significant bit(LSB) to Most significant bit(MSB). The Carry select adder is one of the adder architectures that reduces the carry propagation delay by grouping sub-block of adders. Many techiques can be used to improve the CSA performance as proposed by researchers in previous work that is, by using BEC-1(Binary to eccess-1 converter), using D-Latch etc. In this work, the CSA is designed using GDI(Gate diffusion input) technique and using both GDI and MTCMOS D-Latch to achieve better performance as compared to previous work. Mentor Graphics 130nm CMOS Technology is used for simulation. The design of CSA using Both GDI and MTCMOS logic achieved a tremendous improvement in operation speed, power consumption and Transistor count of 92.7%, 99.45% and 58.85% respectivelly as compared to the conventional CSA.

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A review of 0.18-/spl mu/m full adder performances for tree structured arithmetic circuits
IEEE Transactions on Very Large Scale Integration (VLSI) Systems
Published: 2005

High-speed low-power adder with a new logic style: pseudo dynamic logic (SDL)
ICM 2001 Proceedings. The 13th International Conference on Microelectronics.
Published: 2001

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Ombeni Kanze Kennedy
Department of Electronics and Communication Engineering, Aditya Engineering College, Andrapradesh, India

G. SRIDEVI
Department of Electronics and Communication Engineering, Aditya Engineering College, Andrapradesh, India

Contents

Over the last few decades, phenomenal growth has occured in the electronic industry mainly due to rapid advances in the large-scale system design and integration technologies [1]. For high-performance and other scintific and engineering applications, digital CMOS ICS have been the driving force behind very-large-scale-integration(VLSI) [1]. The use of integrated circuits in high-performance computing, consumer electronics and Telecommunications has grown at a very fast pace. The driving force for the fast developement of this field is typically, the required information and computational power of these applications. Although the Ripple carry adder is the simplest multi-bit adder architecture, the carry signal delay will increase significantly when the number of bits is increased to 32 or 64 bits [1].

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Ombeni Kanze Kennedy
Department of Electronics and Communication Engineering, Aditya Engineering College, Andrapradesh, India

G. SRIDEVI
Department of Electronics and Communication Engineering, Aditya Engineering College, Andrapradesh, India

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A compact low cost microstrip Patch antenna(MPA) is proposed in this paper. The overall size of the proposed antenna measures 21mm x 14 mm x 1.6 mm. The simulation and analysis is done using CST Microwave Studio. The antenna parameters such as Bandwidth, input impedance, VSWR, Efficiency, Gain and Radiation pattern are simulated and analysed. The antenna resonates at wide frequency band from 3.11 to 14.254 GHz. Hence, achieving a bandwidth of 11.14GHz and a fractional bandwidth of 128.31%. The antenna is more efficient in the Ultra wide-band frequency band from 3.1 to 10.6 GHz with an average efficiency of 68 percent. The antenna is designed on a low-cost FR-4 substrate which is easily available on the market. The simulated results show that the proposed antenna has a wide range of applications such as WIMAX(3.4 to 3.6 GHz and 3.7 to 4.2 GHz), WIFi 802.11y(3.6 to 3.7), S-band(2 to 4GHz), C-band(4 to 8 GHz), X-band(8 to 12GHz), Ku-band(11.7 to 12.7GHz for downlink).

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A microstrip-fed ultra-wideband antenna with dual band-notch characteristics
2016 39th International Conference on Telecommunications and Signal Processing (TSP)
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Slit Loaded Circular Ultra Wideband Antenna for Band Notch Characteristics
2019 National Conference on Communications (NCC)
Published: 2019

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I. Introduction

In wireless communication systems, one of the main objectives is the design of wide-band, or even multiband, low profile, small antennas. Applications of such antennas include, but are not limited to, personal communication systems, small satellite communication terminals, unmanned aerial vehicles, and many more.

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In this paper, it was proposed to measure the leakage current experimentally on four samples of polymeric and porcelain insulators of 132kV with and without some practically available pollutants in the environment such as salt, urea and cement etc. and also compared the performance of both type of insulators when different pollutions are present on the insulator surface. The experimental analysis shows that the leakage current was more in porcelain insulator when compared with polymeric insulator. But in this experiment we observed that, the leakage current in Urea coated Porcelain insulator was more than the urea coated Polymeric insulator.

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2006 IEEE 8th International Conference on Properties & applications of Dielectric Materials

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S Sudhakar Rasamsetti
EEE Department, Aditya Engineering College(A), India

N Sumathi
EEE Department, JNTUK, Kakinada, India

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I. Introduction

Ever since man was able to generate electricity in significant quantity (circa 1880), sufficiently robust insulators have been used for power transportation [1]. Polymer insulators were first developed in the 1950s to replace conventional ceramic insulators. They were not, however, available until the 1960s because of initial design flaws. These insulators are generally constructed of fiberglass reinforced polymer rods and a polymer housing. Developed in Europe, the first polymer insulators produced flashover, tracking, and general line drop problems due to flaws that developed in the polymers that were used. The high voltage insulators eventually succumbed to cracking or shedding of the polymer housing, known as chalking [2].

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S Sudhakar Rasamsetti
EEE Department, Aditya Engineering College(A), India

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ISCAS 2001. The 2001 IEEE International Symposium on Circuits and Systems (Cat. No.01CH37196)

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In VLSI system, the integrated circuit design has modest importance. The important parameters considered for the design of the circuit are power, delay, area and complexity of the circuit. Binary adder is the fundamental element in the digital circuit design viz., multipliers and digital signal processors. Nowadays, extensive research is focused on reducing the power consumption, and delay in the computation. There are different types of adders, but these are not dominant in terms of propagation delay. The adder with less time for computation is preferred in such a high speed applications. So, in order to optimize the delay, parallel prefix adders like Kogge Stone Adder is preferred. It is the fastest adder which focuses on design time and is said to be a good alternative for high performance applications. The speedy nature of Kogge Stone Adder (KSA) is because of minimum logic depth and restricted fan-out. In KSA, parallel advance will give scope to generate fast carry for intermediate stages. Each level generates Propagation Generation (PG) blocks simultaneously. Among all types of 64 bit adders, a KSA has less delay (11.37ns). In this work, a 64 bit GDI logic based KSA schematic is designed by using Mentor Graphics EDA Tool in 130nm Technology. Performance parameters like delay, average power consumption (at various dimensions of

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Bujjibabu Penumutchi
Dept. of ECE, AEC

Satyanarayana Vella
Dept.of ECE, AEC

Harichandraprasad Satti
Dept.of ECE, AEC

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An adder is a digital circuit used to get summation as output from the given inputs. In computers and other kinds of processors these summing networks are used in the arithmetic logic units.

Besides, they are also used to calculate addresses, table indice, increment, and decrements operations. The adders can be constructed for different number representations, such as binary-coded decimal or excess-3. The most common adders operate on binary numbers. Though many adders are available, the selection of adder will be based on parameters, viz. area, power consumption and time of computation

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Authors

Bujjibabu Penumutchi
Dept. of ECE, AEC

Satyanarayana Vella
Dept.of ECE, AEC

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Dept.of ECE, AEC

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Characterization and spectroscopic studies of multi-component calcium zinc bismuth phosphate glass ceramics doped with iron ions

AIP Conference Proceedings 1942, 070014 (2018); https://doi.org/10.1063/1.5028812

A. Suneel Kumar[1], T. Narendrudu[2], S. Suresh[3], G. Chinna Ram[1], M. V. Sambasiva Rao[1], Ch. Tirupataiah[1], *and* D. Krishna Rao[1,a)]

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[1]Department of Physics, Acharya Nagarjuna University, Nagarjuna Nagar - 522510, A.P., India
[2]Department of Physics, Aditya Engineering College, Surampalem-533437, A.P., India
[3]Department of Physics, Gudlavalleru Engineering College, Gudlavalleru-521356, A.P., India
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Role of valence state of vanadium ions on structural and spectroscopic properties of sodium lead bismuth silicate glass ceramics

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M. V. Sambasiva Rao[1,a)], Ch. Tirupataiah[1], A. Suneel Kumar[1], T. Narendrudu[2], S. Suresh[3], G. Chinna Ram[1], *and* D. Krishna Rao[1]

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[2]Department of Physics, Aditya Engineering College, Surampalem-533437, A.P., India
[3]Department of Physics, Gudlavalleru Engineering College, Gudlavalleru-521356, A.P., India
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Arithmetic operations play a crucial role in signal processing applications, micro processors, and micro controllers. Multiplication operation is widely used in Digital Signal Processing (DSP) modules like Infinite Impulse Response (IIR) filters, Finite Impulse Response (FIR) filters, Discrete Fourier Transform (DFT), Fast Fourier Transform (FFT), Discrete Cosine Transform (DCT) and etc. Existed design generating partial products using RADIX-4 Modified Booth Encoding (MBE) and partial products addition is done by using Wallace tree approach with Carry Save Adder (CSA). Now we modify above design, RADIX-4 MBE is replaced with RADIX-8 MBE for partial products generation and Wallace CSA tree is replaced with CLA tree for partial products addition. In both designs pipelining technique is involved. Performance comparison between existed RADIX-4 pipelined multiplier and RADIX-8 pipelined multiplier with above addition approaches, the modified method yields considerable moderate critical path delay, area and 35% reduced the power consumption. Modified design is implemented in XILINX 14.7 with FPGA technology XC3S500E-FG320-5.

Published in: 2017 2nd International Conference on Communication and Electronics Systems (ICCES)

Date of Conference: 19-20 October **INSPEC Accession Number:**

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The Effect of Multi-Bit Correlation on the Design of Field-Programmable Gate Array Routing Resources

IEEE Transactions on Very Large Scale Integration (VLSI) Systems

Published: 2011

Some modular adders and multipliers for field programmable gate arrays

Proceedings International Parallel and Distributed Processing Symposium

Published: 2003

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I. Introduction

A binary multiplier is an electronic circuit used in digital electronics, such as a computer, to multiply two binary numbers. It is built using binary adders. A variety of computer arithmetic techniques can be used to implement a digital multiplier. Advanced consumer electronics make wide use of Digital Signal Processing (DSP) providing accelerators for the domains of communications, general, military purpose systems. In DSP applications carry out a large number of arithmetic operations as their implementation based on computationally intensive kernels, such as Discrete Fourier Transform (DFT), Fast Fourier Transform (FFT), Infinite Impulse Response (IIR) and Finite Impulse Response (FIR). DSP system performance can be evaluated by the design allocation and architecture of arithmetic units. Recent research activities in the field of optimized arithmetic operations are grown up. Data transfer in different digital modules is done by the arithmetic operations (sub modules). One of the important sub modules is multiplier. Different multiplier designs were introduced to enhancing more efficient implementations of DSPalgorithms. Severalapproacheshavebeenproposedtooptimiz etheperformanceof the multiplier operation in terms of area, power consumption. This can be done by placing of arithmetic units like multiplier Many DSP applications can be implemented based on multiplier operation.

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Authors

Vadapalli SivaCharanKumar
ECE Department, Aditya Engineering College, Andhrapradesh

Penumatchi Bujjibabu
ECE Department, Aditya Engineering College, Andhrapradesh

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Abstract:

Cloning (copy-move forgery) is a malicious tampering attack with digital images where a part of image is copied and pasted within the image to conceal the important details of image without any obvious traces of manipulation. This type of tampering attacks leaves a big question of authenticity of images to the forensics. Many techniques are proposed in the past few years after powerful software's are developed to manipulate the image. The proposed scheme is involved with both the block based and feature point extraction based techniques to extract the forged regions more accurately. The proposed algorithm mainly involves in matching the tentacles of same features extracted from each block by computing the dot product between the unit vectors. Random Sample Consensus (RANSAC) algorithm is used to extract the matched regions. The experimental result of the algorithm which is proposed indicates that, it can extract more accurate results compared with existing forgery detection methods.

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Gonapalli Ramu
Aditya Engineering College, Surampalem, Kakinada

S. B. G. Thilak Babu
Aditya Engineering College, Peddapuram, Andhra Pradesh, IN

Contents

Authors

Gonapalli Ramu
Aditya Engineering College, Surampalem, Kakinada

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A Lossy Compression Approach of Compressing Encrypted Images

S.V.V.D.Jagadeesh[1], K. Raja Sravan Kumar[2]

[1,2]*Dept. of IT, Aditya Engineering college., Surampalem, E.G.dt,AP, (India)*

ABSTRACT

In this paper proposing a novel scheme of compressing encrypted images. In the encryption phase, the original pixel values are masked by a modulo-256 addition with nonrandom numbers that are derived from a secret key. After decomposing the encrypted data into a down sampled subimage and several data sets with a multiple-resolution construction, an encoder calculates the subimage and the Hadamard coefficients of each data set to reduce the data amount. Then, the data calculates subimage and coefficients are regarded as a set of bitstreams. Because of the hierarchical coding mechanism, the principal original content with higher resolution can be reconstructed when more bitstreams are received.

Keywords:Hadamardtransform, image compression, image encryption, scalable coding.

I.INRODUCTION

In recent years, encrypted signal processing has motivated to considerable research interests [1]. The discrete Fourier transform and adaptive filtering can be implemented in the encrypted domain based on the homomorphic properties of a cryptosystem [2], [3], and a composite signal representation method can be used to reduced the size of encrypted data and computation complexity [4]. In joint encryption and data hiding, a part of significant data of a plain signal is encrypted for content protection, and the remaining data are used to carry the additional message for copyright protection [5], [6]. With some buyer–seller protocols [7], [8], the fingerprint data are embedded into an encrypted version of digital multimedia to ensure that the seller cannot know the buyer's watermarked version while the buyer cannot obtain the original product on template base process. A number of works on compression encrypted images have been also presented. When a sender encrypts an original image for privacy protection, a channel provider without the knowledge of a cryptographic key and original content may be given to reduce the data amount due to the limited channel resource. In [9], the compression of encrypted data is looked into with the theory of source coding with side information at the decoder, and it is pointed out that the performance of compressing encrypted data may be as good as that of compressing non-encrypted data in theory. Two practical approaches are also given in [9]. In the first one, the original binary image is encrypted by adding a pseudorandom string, and the encrypted data are compressed by finding the syndromes of *low-density parity-check* (LDPC) channel code. In the second one, the original Gaussian sequence is encrypted by adding an independent identically distributed Gaussian sequence, and the encrypted data are quantized and compressed as the syndromes of trellis code. While Schonberg *et al.* [10] study the compression of encrypted data for memoryless and hidden Markov sources using LDPC codes, Lazzeretti and Barni [11] present several lossless compression methods for encrypted gray and color images

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REVIEW OF GAS TURBINE BLADES

Mohammad Hussain[1], P.Harichandra Prasad[2], K Prudhvi Ravikumar[3]

1 Assistant Professor, Aditya Engineering College ,Surampalem
[2]Assistant Professor, Aditya Engineering College ,Surampalem
[3]Assistant Professor, Aditya Engineering College ,Surampalem

HIGHLIGHTS:

The different cooling systems used for cooling turbine blade.
Methods adopted for the design of turbine blades.
Loads effecting the performance of the turbine blade.
Different coating materials preferred for protecting the blade.

ABSTRACT

Now a day's gas turbine engines have skills a couple of application ranging from land headquartered vigour vegetation to ship and plane propulsions for the period of the last decades the research carried out on the blades ended in the design of engine with the potential to sustain higher combustion temperatures, as a consequence acquiring a huge augmentation of efficiency and efficiency .These success have been possible more often than not by the use of novel materials and by way of the development of more effective systems. A turbine blade is the individual aspect which makes up the turbine element of a gas turbine .The blades are liable for extracting vigour from excessive temperature, excessive pressure fuel produced by way of the combustion. Extraordinary parameters which impact the execution of blades are coating substances, cooling techniques; channels made on the blade are studied in the paper and the popular stipulations to conquer these challenges like the life time of the blade, immoderate oxidization and erosion, and the thermal stress. The assessment paper gives the transient suggestion related to the turbine blades and explanations to decide upon turbine blade for required purpose.

Keywords: gas turbine blades, cooling system, coatings, blade loads, blade Design.

1.INTRODUCTION

1.1 Cooling systems

1. Gas plants are being viewed to develop as the essential alternative for future power emphasis strategies, because of the reality of their high fuel change successfully and brought down energy new discharge expense the present cooling procedures for high strain gas turbine sharp edges involve a combo of interior cooling (constrained convection impingement) and outside (film cooling) arrangement

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Comparative analysis of multi carrier PWM eleven level inverter with two modulation waves

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Abstract:

Multilevel Inverter is introduced to reduce the switching stress and to obtain the output voltage with multiple steps to achieve the lowest total harmonic distortion (THD) and improved fundamental VRMS. This paper presents comparison of various methods used for reduction of THD and for improving VRMS. An eleven inverter is triggered by using Bipolar Multicarrier Pulse Width Modulation method, sine and Trapezoidal Amalgamated Rectangular (TAR) references with triangular carriers. There are seven various types of triangular carriers. They are, Phase Disposition, Phase Opposition Disposition, Alternate Phase Opposition Disposition, Carrier Overlapping, Phase Shift and Variable Frequency methods. The Performances measure like, THD, VRMS are evaluated for various modulation indices. Simulation is carried out by using MATLAB/SIMUINK. It is observed that sine reference based PWM method provides lower THD, TAR reference based PWM method provides higher fundamental VRMS output voltage.

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B. V. V. L. Kala Bharathi
Department of Electrical and Electronics Engineering Aditya Enginering College, Surampalem Kakinada, India

V. Srinivasa Rao

Department of Electrical and Electronics Engineering, Aditya Enginering College, Kakinada, India

Contents

In the present day scenario private power producers are increasing rapidly to meet the increased demand. In this process, the existing transmission lines are overloaded and lead to unstable system. Due to the meshed topology of transmission lines and the multiplicity of equipment, the planning and operation of power systems have become very complex. Complex studies have been carried out on normal and abnormal performances of a power system, and also in the present and future functioning of the electrical energy system. One of the abnormal performances of electrical energy transmission systems refers to the occurrence of contingencies. The contingency analysis is very important when future conditions are uncertain. Thus, contingency based planning reflects good energy management practices and helps to create more resilient power systems. Also, it tends to reduce costs, improve energy efficiency, and expand the range of possible solutions compared with more rigid planning.

Authors

B. V. V. L. Kala Bharathi
Department of Electrical and Electronics Engineering Aditya Enginering College, Surampalem Kakinada, India

V. Srinivasa Rao
Department of Electrical and Electronics Engineering, Aditya Enginering College, Kakinada, India

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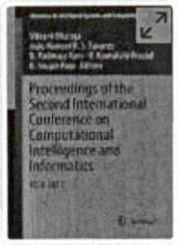

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An Agile Effort Estimation Based on Story Points Using Machine Learning Techniques

Ch. Prasada Rao ✉, P. Siva Kumar, S. Rama Sree & J. Devi

Conference paper | First Online: 24 July 2018

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Nowadays, many software companies face the problem of predicting the accurate software effort. Most of the software projects are failed due to over budget and over schedule as well as under-budget and under-schedule. The main reason for the failure of software projects is inaccurate effort estimation. To improve the accuracy of effort estimation, various effort estimation techniques are introduced. Functional points, object points, use case points, story points, etc., are used for effort estimation. Earlier, traditional process models like waterfall model, incremental model, spiral model, etc., are

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Author information

Authors and Affiliations

K L University, Vaddeswaram, Guntur, India

Ch. Prasada Rao & P. Siva Kumar

Aditya Engineering College, Surampalem, India

S. Rama Sree & J. Devi

Corresponding author

Correspondence to Ch. Prasada Rao .

Editor information

Editors and Affiliations

Department of Electronics and Communication Engineering, Shri Ramswaroop Memorial Group of Professional Colleges, Lucknow, Uttar Pradesh, India

Prof. Dr. Vikrant Bhateja

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Dr. B. Padmaja Rani

Department of Computer Science and Engineering, JNTUH College of Engineering Hyderabad (Autonomous), Hyderabad, Telangana, India

Dr. V. Kamakshi Prasad

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Smart Intelligent Computing and Applications pp 559–569

PSO Algorithm Support Switching Pulse Sequence ISVM for Six-Phase Matrix Converter-Fed Drives

Ch. Amarendra ✉ & K. Harinadha Reddy

Conference paper | First Online: 02 October 2018

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Abstract

A matrix converter (MC) is an array of power electronic switches that are directly connected from input to output. The six-phase matrix converter (SPMC) is an advanced power electronic converter having three-phase input and six-phase output. The SPMC provides the six-phase output for the six-phase applications. In this paper, the SPMC is operated with the indirect space vector modulation (ISVM). This ISVM is unable to bring the harmonic content below standard value. The value of harmonics should be less than 5% as per the standard IEEE value. The optimization technique is able to reduce the harmonic content in the output

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Space vector control of 5-phase PMSM supplied by 5 H-bridge VSIs. In: Conference on Modeling and Simulation of Electric Machines, Converters and Systems (ElectrIMACS'02), Montreal, Canada (2002)

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Author information

Authors and Affiliations

Department of EEE, Koneru Lakshmaiah Education Foundation, Vaddeswaram, Guntur, AP, India

Ch. Amarendra

Department of EEE, Lakireddy Bali Reddy College of Engineering (A), Mylavaram, Krishan District, AP, India

K. Harinadha Reddy

Department of EEE, AEC, Surampalem, AP, India

Ch. Amarendra

Corresponding author

Correspondence to Ch. Amarendra .

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Editor information

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School of Computer Engineering, KIIT Deemed to be University, Bhubaneswar, Odisha, India

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