ADITYA ENGINEERING COLLEGE

An Autonomous Institution

Approved by AICTE • Permanently Affiliated to JNTUK • Accredited by NAAC with 'A' Grade

Recognised by UGC under sections 2(f) and 12(B) of UGC Act, 1956

Aditya Nagar, ADB Road, Surampalem - 533437, Near Kakinada, E.G.Dt., Ph:99498 76662

Department of Electronics and Communication Engineering

Date: 16.11.2021

Report on

"Digital Design using Cadence Tool"

Name of the Event: Training programme on Digital Design using Cadence Tool

Introduction to Event:

This programme was organised by the department of ECE to make the students learn how to design digital system with considering design metrics. Designs are getting bigger and more complex. This translates to more challenging power, performance, and area (PPA) targets. It's a tall engineering order to meet, made tougher with schedules that continue to shrink. The Cadence integrated digital full flow offers innovations that go across individual tool boundaries through the integration of core engines and key technologies. Using the Cadence digital full flow, customers can beat their PPA goals ahead of schedule. Early simulation and primitive hardware generation tools have given way to sophisticated design entry, verification, high-level synthesis, formal verification, and automatic hardware generation and device programming tools. In order to meet the current trends in electronic design industry, students need to equip with the basic knowledge of digital design flow using Cadence tool. Keeping this in view, the department has organized this training programme for the benefit of the students.

Event Dates:09-11-2021to 13-11-2021

Number of Days:5 days

Co-ordinator: Mr.T.Srinivasa Rao,Assoc.Professor, Department of ECE.

Agenda:

Day-1: Introduction to Digital System Design

Day-2: Behavioral and RTL models of digital circuits

Day-3: Verification of RTL models

Day-4:FSM-basedDigital Design

Day-5:Features of Standard Cell Libraries and FPGAs

No. of Participants: 180

Experts with Designation:

1. Rajiv Vk, Senior Director, Test Engineering at Tessolve Semiconductor Pvt.Ltd.
2. Dhanya Menon, Technical Trainer at Tessolve Semiconductor Pvt. Limited

Venue: Cotton Bhavan Seminar Hall (Room No: 208)

Hospitality/Accommodation: Yes

Staffing:

1. Mrs.B.S.Sridevi, Assoc. Professor
2. Ms.Ch.V.Kiranmai, Asst.Professor

Outcomes:

- Students have become familiarized with the modern design flow for digital circuits and the relevant software tools
- Students were able to apply the knowledge gained in the design of complex digital circuits

Conclusive Remarks:

The objective of this programme, imparting knowledge on digital system design flow is fulfilled. Students learnt the digital system design concepts. This learning experience covered a wide breadth of topics from the key steps involved in system design to how to maximize its performance besides reducing the area and delay. This training showcased a wide variety of examples to illustrate the key points in designing a digital system.

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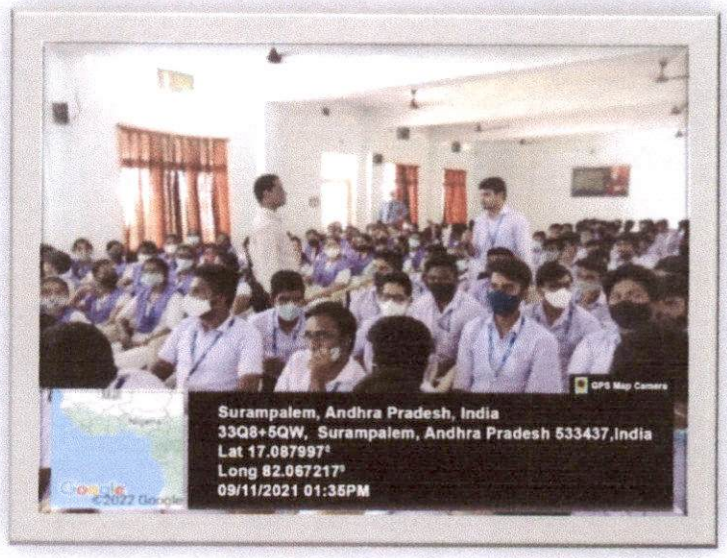
"Digital Design using Cadence Tool"

Inaugural session on 09/11/2021



Presentation session on 09/11/2021

Presentation session on 11/11/2021

Interactive session on 13/11/2021

Coordinator

PRINCIPAL
ADITYA ENGINEERING COLLEGE
SURAMPALEM - 533 437

Head of the Department

Head of the Department
Department of E.C.E.
Aditya Engineering College (A9)