

ADITYA ENGINEERING COLLEGE (A)

Aditya Nagar, ADB Road - Surampalem

LESSON PLAN

Academic Year
2021-22

Year & Sem. : B.Tech.- VI Sem.

Branch : ECE

Course : VLSI DESIGN

Date	Topic to be covered	Mode of Teaching	No. of Periods
I WEEK 14-02-2022 to 19-02-2022	UNIT-I: Introduction: Introduction to IC Technology	PPT	1
	MOS and related VLSI Technology	PPT	1
	Basic MOS Transistors	PPT	1
	Enhancement & Depletion mode of transistor action	PPT	1
II WEEK 21-02-2022 to 26-02-2022	IC production process	Video Demonstration	1
	MOS & CMOS Fabrication processes	PPT	1
	Bi-CMOS Technology	Brain Storming	1
	Comparison between CMOS and Bipolar technologies	PPT	1
III WEEK 28-02-2022 to 05-03-2022	01-03-2022 - Maha Shivarathri		
	UNIT-II: Basic Electrical Properties of MOS and Bi-CMOS Circuits: I_{ds} versus V_{ds} Relationships	Chalk and talk	1
	Aspects of MOS transistor: Threshold Voltage	Inquiry-Based Learning	1
	MOS transistor Transconductance, Output Conductance	Chalk and talk	1
	Figure of Merit, The Pass transistor	Chalk and talk	1
IV WEEK 07-03-2022 to 12-03-2022	NMOS Inverter	PPT	1
	Pull-up to Pull-down Ratio for NMOS inverter driven by another NMOS inverter	Chalk and talk	1
	Pull-up to Pull-down Ratio for NMOS inverter driven by another NMOS, Alternative forms of pull-	Chalk and talk	1
	The CMOS Inverter, MOS transistor circuit model	Assignment	1
V WEEK 14-03-2022 to 19-03-2022	18-03-2022 - Holi		
	Bi-CMOS Inverter, Latch-up in CMOS circuits and Bi-CMOS Latch-up Susceptibility	PPT	1
	Transistor switches, Schematics of Inverter, NAND, NOR gates using	Chalk and talk	1
	Schematics of Inverter, NAND, NOR gates using PMOS technology	Chalk and talk	1
	Schematics of Inverter, NAND, NOR gates using CMOS technology	Simulation-based learning	1
VI WEEK 21-03-2022 to 26-03-2022	UNIT-III: MOS and Bi-CMOS Circuit Design Processes: MOS Layers	Chalk and talk	1
	Design Rules	PPT	1
	General observations of design rules	PPT	1
	General observations of design rules	PPT	1
VII WEEK 28-03-2022 to 02-04-2022	02-04-2022 - Ugadi		
	NMOS Circuit stick diagram for inverter	PPT	1
	NMOS Circuit stick diagrams for NAND and NOR	PPT	1
	NMOS Circuit layout diagram for inverter	PPT	1
	NMOS Circuit layout diagrams for NAND and NOR	PPT	1

Sub
PRINCIPAL
Aditya Engineering College
SURAMPALAM

VIII WEEK 04-04-2022 to 09-04-2022	I Sessional Exams		
IX WEEK 11-04-2022 to 16-04-2022	14-04-2022 - Dr.B.R.Ambedkar's Birth Day		
	15-04-2022 - Good Friday		
	CMOS Circuit stick diagram for inverter	PPT	1
	CMOS Circuit stick diagrams for NAND and NOR	PPT	1
X WEEK 18-04-2022 to 23-04-2022	CMOS Circuit layout diagram for inverter	PPT	1
	CMOS Circuit layout diagrams NAND and NOR	PPT	1
	2 μ m Double Metal, Double Poly, CMOS/Bi-CMOS rules	PPT	1
	1.2 μ m Double Metal, Double Poly CMOS rules	Chalk and talk	1
XI WEEK 25-04-2022 to 30-04-2022	Symbolic Diagrams-Translation to Mask Form.	Chalk and talk	1
	UNIT-IV:Basic Circuit Concepts: Sheet Resistance	Chalk and talk	1
	Sheet Resistance concept applied to MOS transistors& Inverters	Chalk and talk	1
	Area Capacitance of Layers, Standard unit of capacitance	PPT	1
XII WEEK 02-05-2022 to 07-05-2022	Inverter Delays, Propagation Delays	PPT	1
	03-05-2022 - Ramzan(Eid-ul-Fitr)		
	Wiring Capacitances, Fan-in & fan-out, Choice of layers	Chalk and talk	1
	Scaling of MOS Circuits:Scaling models,Scaling factors	PPT	1
XIII WEEK 09-05-2022 to 14-05-2022	Subsystem Design: Architectural issues, switch logic	PPT	1
	Gate logic	PPT	1
	Examples of structured design	PPT	1
	Clocked sequential circuits, system considerations	PPT	1
XIV WEEK 16-05-2022 to 21-05-2022	Illustration of design processes	PPT	1
	UNIT-V:VLSI Design Issues: VLSI Design issues and design trends	Guest Lecture	1
	Technology options,power calculations, package selection	PPT	1
	Clock mechanisms	Video Demonstration	1
XV WEEK 23-05-2022 to 28-05-2022	Mixed signal design, ASIC design flow	PPT	1
	Introduction to SoC design	PPT	1
	Over view on DFT	Workshop	1
	FPGA Design: Basic FPGA architecture,FPGA configuration, configuration modes	PPT	1
XVI WEEK 30-05-2022 to 04-06-2022	FPGA design process- FPGA design flow, FPGA families	PPT	1
	II Sessional Exams		
Total number of classes			54

Y. Yamini
Course Coordinator

S.M.
PRINCIPAL
Aditya Engineering College
SURAMPALAM

A. Sridhar
Head of the Department